**# Single Board Computer for 6502**

**\*\*with Virtual Memory Kernal and Memory Management Unit\*\***

*\*A lifelong learning experience ...\**

The Single Board Computer for 6502 is an amateur project to explore and understand the computer science topics around multi-tasking operating systems and virtual memory hardware.  The 6502 processor was chosen for its software and hardware simplicity.  And as a nod to the KIM-1 used in my undergraduate work.  All design decisions lean towards simplicity and implementing minimum needed to research the stated topics.

The Virtual Memory Kernal (VMK) and Memory Management Unit (MMU) will support:

•   Multi-Tasking – More than one process in memory at a time.

•   Preemptive Tasking – Prosses are interrupted to allow other processes access to computer resources.

•   Kernel Mode – Processes may run in a protected mode allowing access to all computing resources.

•   Virtual Memory – Processes are run in a continuous virtual 64KB memory environment.

The Single Board Computer for 6502 (SBC6502) will have the following characteristics:

•   A 20-bit 1MB address space divided into 512KB RAM, 32KB ROM and 16KB memory mapped I/O.

•   The MMU will support up to 4KB virtual memory pages.

•   All primary computer logic (MMU, memory decoding, etc.) will be implemented with 7400 series ICs.

•   Arduinos will be used to implement complex I/O devices such as video and serial communication.

**## Overview**

The 6502 is an 8-bit processor with a continuous 16-bit 65KB memory model.  Sections of the address space a proportioned off for the Zero Page (256 bytes), Stack (256 bytes) and interrupt vectors (6 bytes).  The goal of the VKM and MMU will be to present the full 64KB memory model to each process.  The Configuration Registers (CR0 & CR1) are programmable at boot time and set how the MMU will function.

The MMU has 2 memory-mapped configuration registers that control:

\* The number of effective memory bits; the total address space of the SBC6502

\* The number of bits in a Procss ID (PID)

\* The size of each memory page

\* The number of process bits used to address a page segment

The MMU provides a protected Kernal Mode by intercepting BRK and RTI instrucions.